# KLayout – Mask lay-out design

Available from: <http://www.klayout.de/build.html> for Windows, Mac and Linux. This manual has been written around version 0.26.10.

KLayout is a free mask editing program which we will use to edit the so-called GDSII files (\*.gds) from the photolithography masks which will be used during the fabrication. GDSII is an international standard to submit mask data, a process called taping out as in the past masks where submitted on cassette tapes due to the large amount of data.

Start-up and changing the group name

1. Start KLayout **(Editor)**. Be sure to start the editor version and *not* the default or viewer mode!Annoyingly, KLayout has three icons in the Start Menu of Windows, and the only one useful for us is the icon KLayout (Editor). If you have trouble getting it to start in editing mode go to File – Setup, Applicating – Editing Mode and enable ‘Use editing mode by default’.
2. **Do not use Ctrl + S to save, this does something completely different in KLayout**
3. Open GroupXYZ.gds, where *xyz* should be changed before in your **unique** group number before opening. E.g., Group001.gds.
4. Under File – Load Layer Properties – load the file EKL-tech.lyp, this will change the names and colours of the layers to facilitate easy drawing
5. In the cell box on the left of the screen, change the name of the cell from groupXYZ into your unique group number by right clicking on the name and choosing *Rename Cell* (e.g., group001)
6. Go to Display – Full Hierarchy, this should make the text visible.
7. Select the ‘Group XYZ’ text in the chip, select ‘Q’ and edit the name in the Text field to your group number.
8. You should now see the screen in figure 8.

Design rules, and design rule check

The models used to simulate the transistor are extracted from a specific process and are only valid in a certain range of device geometries. The fabrication process itself is fixed and as designer you have typically no influence on the process parameters that the semiconductor foundry uses. You can only change the geometry of the devices. However, to ensure that the process results in physically working devices and valid models, you as designer will have to follow a set of rules during the design process. **Deviating from these rules can result in devices which do not work properly or at all!**

On the next page are the design rules for our custom-CMOS process that will be fabricated in the Else Kooi Laboratory of the TU Delft. **Read them before you start drawing and use them during the design, and after you are done carefully check every single one of them and confirm these are correct.** This Design Rule Check (DRC) is normally performed automatically for a complex circuit.

|  |  |
| --- | --- |
| General design rules | Ok? |
| Minimum feature size: 2 µm (due to use of a contact aligner), step size: 1 µm |  |
| No features may be placed outside the cell outline |  |
| No other features except 90 degrees corners can be drawn (no circles), only the IC layer can also have 45-degree corners |  |
| The maximum chip area is 3x3 mm |  |
| The cell name is changed to include the group number instead of XYZ |  |
| The group number has been written on the chip |  |
|  |  |
| SN specific rules (source, drain, resistor) |  |
| Minimum width ≥ 2 µm |  |
| Minimal separation (channel length) between source and drain ≥ 2 µm |  |
|  |  |
| SP specific rules (guard ring) |  |
| Minimum width ≥ 2 µm |  |
| No overlap with SN allowed; minimum separation ≥ 5 µm, max ≤ 20 µm |  |
| All SP areas should be connected to the ground pad |  |
|  |  |
| CO specific rules (contact openings) |  |
| Minimum size ≥ 2x2 µm |  |
| SN or SP area should be at least 3 µm larger around the CO hole |  |
| All SN and SP areas should have at least one CO |  |
| No CO allowed to un-doped Si areas |  |
| Only squares or rectangles allowed |  |
|  |  |
| IC specific rules (interconnect) |  |
| Minimum width ≥ 4 µm |  |
| The entire channel is covered by IC (gate IC) |  |
| The gate IC covers the SN around the channel by 2 µm |  |
| IC should be ≥ 3 µm larger than CO |  |
| Every CO has an IC on top |  |
| Different IC lines are ≥ 3 µm apart |  |
| Different IC lines cannot cross each other (short-circuit!) |  |
| Contact pads are 1x1 mm and cannot be changed or moved |  |
| Contact pads lay 300 µm from the chip edge |  |
| Text is in the IC layer, min size 100 (template uses 150) |  |
|  |  |
| Outline layer (not fabricated, but required for merging designs) |  |
| Nothing, except a 3x3 mm box, is drawn using the Outline layer |  |
| No structures are drawn outside the 3x3 mm outline layer |  |
| The outline box is 3x3 mm and centred, select box, and press ‘Q’ to check |  |

Moving around

You can move around using the arrow keys and zoom in and out using the scroll wheel or by pressing enter and shift + enter for zooming out. You will zoom at the location where your cursor is. To go back to the overview of your chip, use F2 to ‘Zoom Fit’.

Editing the lay-out

**Important:** to make drawing much easier you can adjust the snapping grid: ‘F3’ under Snapping for the Grid field, select ‘Other grid ..’ and fill the snapping grid (e.g. ‘1’ for 1 µm). To prevent the drawing of anything except horizontal, vertical, and diagonal lines, ‘Diagonal’ can be selected under Angle Constraints. Remember that only the IC layer can have 45-degree corners, all other layers must have 90-degree corners.

You can draw either boxes or polygons using the tools below the menu bar, although polygons can be tricky. First select on which mask layer you want to draw in the Layer viewer on the right, followed by the tool. Now you can draw on the grid. If you do not see any drawing tools, you did not open KLayout in Editing mode!

Already drawn objects can be moved using the *Move tool*. If you want to edit a single side of an already drawn box, you can use the *Partial tool*. They can also be edited manually by double-clicking on them or pressing ‘Q’. You can delete boxes by selecting them and pressing ‘Del’.

You can temporarily hide layers by double-clicking on them in the Layers window.

**Do not draw using the Outline layer, this layer will not be fabricated!**

A screenshot of a computer

Description automatically generated

Figure 8: Main windows of KLayout. The tool bar is below the menu bar. On the left are the cell names, which only contains one cell with your group number. On the right the mask layers can be selected. Drawing is performed in the center.

Adding text

For the testing, it is convenient to add the name of your group to the chip to be able to find the chip after the wafer has been diced easily. This can be done by writing the name using the metal (IC) layer, as this will be the *only* layer that is clearly visible with a magnifying glass.

Drawing the text by hand is cumbersome, luckily the design tool has a function to generate text for you:

1. Select the IC layer.
2. Select the Text element from the toolbar and fill in your group number. Set the text size to 150 and click ‘Apply’ followed by ‘Ok’.
3. Place the text in some free space on your chip, away from the transistor and resistor and bond pads.
4. With the Select tool, select the text by drawing a rectangle around it.
5. Go the Edit – Selection – Convert to PCell, the default name Basic.TEXT is Ok, this will change the text into polygons with the earlier specified size which can be physically put on the chip.
6. If necessary, use the Move tool to correct the position of the text.

Note: in case you cannot see the content of the PCell, go to Display – Full Hierarchy, this should make the polygons visible.

1. Text can be changed by selecting it, pressing ‘Q’ and changing the Text field.
2. You can add more text if you like, but make sure it is not interfering with the devices, or close to the pads and other metal lines.

Finishing and saving the design

If your design matches the dimensions of the simulation and *all* design rules are checked, you can save the file using Save or Save As with your group number. If you get a Save Layout Options window leave all settings default. **Double check that the name of the cell has the group number, and that the file also has your group number!**